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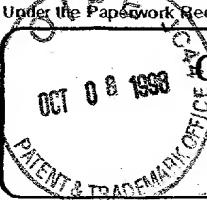
# CONTINUED PROSECUTION APPLICATION (CPA)
# REQUEST TRANSMITTAL

Submit an original, and a duplicate for fee processing.
*(Only for Continuation or Divisional applications under 37 C.F.R. § 1.53(d))*

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| Attorney Docket No. | 1958P1705DIV |
|---|---|
| First Named Inventor | FINK ET AL. |
| Examiner Name | Potter, R. |
| Group / Art Unit | 2508 |
| Express Mail Label No. | EL160875809US |

This is a request for a ☐ continuation or ☒ divisional application under 37 C.F.R. § 1.53(d),

(continued prosecution application (CPA)) of prior application number ___08/644,916___,

filed on __5-24-96__, entitled _A MICROCONTROLLER HAVING AN N-BIT DATA BUS WIDTH_ _WITH LESS THAN N I/O PINS AND A METHOD THEREFOR_

NOTES

*FILING QUALIFICATIONS:* The prior application identified above must be a nonprovisional application that is either: (1) complete as defined by 37 C.F.R. § 1.51(b), or (2) the national stage of an international application in compliance with 35 U.S.C. 371. A Notice will be placed on a patent issuing from a CPA, except for reissues and designs, to the effect that the patent issued on a CPA and is subject to the twenty-year patent term provisions of 35 U.S.C. § 154(a)(2). Therefore, the prior application of a CPA may have been filed before, on or after June 8, 1995.

*CIP NOT PERMITTED:* A continuation-in-part application cannot be filed as a CPA under 37 C.F.R. § 1.53(d), but must be filed under 37 C.F.R. § 1.53(b).

*EXPRESS ABANDONMENT OF PRIOR APPLICATION:* The filing of this CPA is a request to expressly abandon the prior application as of the filing date of the request for a CPA. 37 C.F.R § 1.53(b) must be used to file a continuation, divisional, or continuation-in-part of an application that is not to be abandoned.

*ACCESS TO PRIOR APPLICATION:* The filing of this CPA will be construed to include a waiver of confidentiality by the applicant under 35 U.S.C. 122 to the extent that any member of the public who is entitled under the provisions of 37 C.F.R. § 1.14 to access to, copies of, or information concerning, the prior application may be given similar access to, copies of, or similar information concerning, the other application or applications in the file jacket.

*35 U.S.C. 120 STATEMENT:* In a CPA, no reference to the prior application is needed in the first sentence of the specification and none should be submitted. If a sentence referencing the prior application is submitted, it will not be entered. A request for a CPA is the specific reference required by 35 U.S.C. 120 and to every application assigned the application number identified in such request. 37 C.F.R. § 1.78(a).

1. ☐ Enter the unentered amendment previously filed on _____
   under 37 C.F.R. § 1.116 in the prior nonprovisional application.
2. ☐ A preliminary amendment is enclosed.
3. This application is filed by fewer than all the inventors named in the prior application, 37 C.F.R. § 1.53 (d)(4)
   a. ☐ *DELETE* the following inventor(s) named in the prior nonprovisional application:
   ...................................................................
   ...................................................................
   b. ☐ The inventor(s) to be deleted are set forth on a separate sheet attached hereto.
4. ☐ A new power of attorney or authorization of agent (PTO/SB/81) is enclosed.
5. Information Disclosure Statement (IDS) is enclosed:
   a. ☐ PTO-1449
   b. ☐ Copies of IDS Citations

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[Page 1 of 2]

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PTO/SB/29 (2/98)
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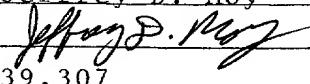
| CLAIMS | (1) FOR | (2) NUMBER FILED | (3) NUMBER EXTRA | (4) RATE | (5) CALCULATIONS |
|---|---|---|---|---|---|
| | TOTAL CLAIMS (37 C F R § 1 16(c) or (l)) | 10 -20* = | -0- | x $ 22.00 = | $ -0- |
| | INDEPENDENT CLAIMS (37 C.F.R §1 16(b) or (i)) | 1 -3** = | -0- | x $ 82.00 = | -0- |
| | MULTIPLE DEPENDENT CLAIMS (if applicable) (37 C.F.R. § 1.16(d)) | | | + $ 270.00 = | -0- |
| | | | | BASIC FEE (37 C.F.R §1 16) | $ 790.00 |
| | | | Total of above Calculations = | | 790.00 |
| | Reduction by 50% for filing by small entity (Note 37 C.F.R. §§ 1.9, 1.27 & 1.28). | | | | |
| | * Reissue claims in excess of 20 and over original patent. ** Reissue independent claims over original patent. | | | TOTAL = | 790.00 |

6. Small entity status:

   a. ☐ A small entity statement is enclosed, if (b) and (c) do not apply.

   b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.

   c. ☐ Is no longer claimed.

7. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 23 - 0830 :

   a. ☐ Fees required under 37 C.F.R. § 1.16.

   b. ☐ Fees required under 37 C.F.R. § 1.17.

   c. ☐ Fees required under 37 C.F.R. § 1.18.

8. ☒ A check in the amount of $ 790.00 is enclosed.

9. ☐ Other: ...........................................................................................

**NOTE:** *The prior application's correspondence address will carry over to this CPA UNLESS a new correspondence address is provided below.*

**10. NEW CORRESPONDENCE ADDRESS**

☐ Customer Number or Bar Code Label

(Insert Customer No. or Attach bar code label here)

or ☐ New correspondence address below

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**11. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED**

| Name (Print /Type) | Jeffrey D. Moy |
|---|---|
| Signature | *Jeffrey D. Moy* |
| Registration No. (Attorney/Agent) | 39,307 |
| Date | |

MTI.1137.US.1

**CERTIFICATE OF MAILING via EXPRESS MAIL**
**37 C.F.R. § 1.10**

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PURSUANT TO 37 C.F.R. § 1.10, I HEREBY CERTIFY THAT I HAVE A REASONABLE BASIS FOR BELIEF THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS EXPRESS MAIL POST OFFICE TO ADDRESSEE, IN AN ENVELOPE ADDRESSED TO:
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ON AUGUST 15, 2001.

RONALD L. CHICHESTER         (REG. NO. 36,765)

**AUGUST 15, 2001**
DATE

**EL905241833US**
EXPRESS MAIL LABEL

| | |
|---|---|
| APPLICATION NUMBER: | 09/522,026 |
| FILING DATE: | OCTOBER 8, 1998 |
| FIRST NAMED INVENTOR: | FINK, ET AL. |
| GROUP ART UNIT: | 2508 |
| EXAMINER: | UNASSIGNED |
| ATTORNEY DOCKET NUMBER: | 068354.0161 |

INCLUDED IN THIS MAILING FOR THE ABOVE-REFERENCED PATENT APPLICATION ARE:
1. CHANGE OF CORRESPONDENCE ADDRESS FOR APPLICATION (PTO/SB/122);
2. POWER OF ATTORNEY;
3. RETURN POSTCARD TO ACKNOWLEDGE RECEIPT OF ABOVE ITEMS.

HOU02:815322.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
  Scott Fink et al.      §
            §
            §   Group Art Unit: 2508
            §
Serial No.: 09/522,026      §   Examiner: R. Potter
            §
Filed: October 8, 1998      §
            §
For:  A Microcontroller Having an N-Bit Data   §
   Bus Width with Less than N I/O Pins    §
   and  Method Therefor       §   Atty Docket: M71462USD1

Office of the Deputy Assistant
  Commissioner for Patent Policy and Projects
Washington, D.C.  20231


Dear Sir:

## PRELIMINARY AMENDMENT

    Applicants hereby submit a Preliminary Amendment for the above-identified patent

application.  Applicants respectfully request that the amendments set forth below be entered

before prosecution on the merits.

## AMENDMENT

In the Claims:

    Please cancel claims 1-10 and add the following new claims:


   -- 11.  A method of operating a microcontroller in an integrated circuit package (IC),

said method comprising the steps of:

    providing an IC chip with a microcontroller having a data bus;

providing a first pin electrically coupled to said microcontroller, wherein said first pin functions as a power supply pin;

providing a second pin electrically coupled to said microcontroller, wherein said second pin functions as a grounding pin; and

providing a plurality of third pins electrically coupled to said microcontroller, wherein said plurality of third pins are function pins, at least one of said plurality of third pins being a multiple function pin, whereby a total number of said first, second and plurality of third pins is at least three which is less than or equal to a bit bus width of said data bus.

12. The method of claim 11, wherein each of said plurality of third pins are one of input only pins or input/output pins.

13. The method of claim 11, further comprising the step of providing at least one configuration circuit coupled to each of said plurality of third pins and to said data bus for determining a function for a corresponding one of said plurality of third pins.

14. The method of claim 13, wherein the step of determining a function for a corresponding one of said plurality of third pins comprises the step of enabling only one at a time of said at least one configuration circuits for each of said plurality of third pins so as to configure a corresponding one of said plurality of third pins to a function associated with said enabled one of said at least one configuration circuits.

15. The method of claim 13, further comprising the step of coupling independent function lines to each of said configuration circuits and to a corresponding one of said plurality

of third pins for transferring data between said corresponding one of said plurality of third pins and said microcontroller when a particular one of said configuration circuits is enabled.

16.    The method of claim 15, further comprising the step of coupling a signal bus to said control register and to said microcontroller for sending signals from said microcontroller to said control register on which of said configuration circuits need to be enabled and which of said configure circuits need to be disabled.

17.    The method of claim 13, further comprising the step of coupling a control register to said data bus for enabling and disabling each of said configuration circuits for determining a function for each of said plurality of third pins.

18.    The method of claim 17, further comprising the step of coupling control signal lines to said data bus and to each of said configuration circuits for transferring to each of said configuration circuits one of said enable and disable signals.

19.    The method of claim 17, wherein said control register is adapted to hold a known logic state.

20.    The method of claim 17, wherein said control register is a memory device.

21.    A method of operating a microcontroller in an integrated circuit package (IC), said method comprising the steps of:

providing an IC chip with a microcontroller having a data bus;

providing a first pin electrically coupled to said microcontroller, wherein said first pin functions as a power supply pin;

providing a second pin electrically coupled to said microcontroller, wherein said second pin functions as a grounding pin;

providing a plurality of third pins electrically coupled to said microcontroller, wherein said plurality of third pins are function pins, at least one of said plurality of third pins being a multiple function pin, whereby a total number of said first, second and plurality of third pins is at least three which is less than or equal to a bit bus width of said data bus;

providing at least one configuration circuit coupled to each of said plurality of third pins and to said data bus for determining a function for a corresponding one of said plurality of third pins, wherein only one of said at least one configuration circuit for each of said plurality of third pins is enabled at a time to configure a corresponding one of said plurality of third pins to a function associated with said one of said at least one configuration circuit which is enabled;

coupling independent function lines to each of said configuration circuits and to a corresponding one of said plurality of third pins for transferring data between said corresponding one of said plurality of third pins and said microcontroller when a particular one of said configuration circuits is enabled;

coupling a control register to said data bus for enabling and disabling each of said configuration circuits for determining a function for each of said plurality of third pins;

coupling control signal lines to said data bus and to each of said configuration circuits for transferring to each of said configuration circuits one of said enable and disable signals; and

coupling a signal bus to said control register and to said microcontroller for

sending signals from said microcontroller to said control register on which of said

configuration circuits need to be enabled and which of said configure circuits need to be

disabled.

22.    The method of claim 21, wherein each of said plurality of third pins are one of

input only pins or input/output pins.

23.    The method of claim 21, wherein said control register is adapted to hold a known

logic state.

24.    The method of claim 21, wherein said control register is a memory device.--


Applicants respectfully request that the amendments below be entered and submit that these

amendments will put the claims in condition for allowance, or in better form for appeal. No new

matter has been entered.    Antecedent basis for the amendments may be found throughout the

specification and drawings as originally filed.

Applicants request reconsideration in light of the amendments and remarks contained

herein.

<div style="text-align:right">

Respectfully submitted,

</div>

DATE:  July 24, 2000                     BY:    _Paul N. Katz_

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ATTORNEY FOR APPLICANTS

# A MICROCONTROLLER HAVING AN N-BIT DATA BUS WIDTH

# WITH LESS THAN N I/0 PINS AND A METHOD THEREFOR

## RELATED APPLICATIONS

This application is a Divisional Application of U.S. patent application Serial Number 08/644,916, filed May 24, 1996 , in the name of the same inventors as the present patent application.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

This invention is in the field of microcontrollers and methods therefor and, more particularly, is a microcontroller having an n-bit architecture (i.e., data bus width) with less than n Input/Output (I/O) pins and a method therefore.

### 2. Description of the Related Art

Microcontrollers are widely known and used in many different applications. A typical architecture used in microcontrollers today is the 8-bit architecture (i.e., the data bus width of the microcontroller is 8 bits wide). One problem with this and other sizes of microcontrollers is that to support an n-bit architecture, greater than n pins are required to be connected to the microcontroller. By reducing the number of pins required to support an n-bit, or more

particularly, an 8-bit microcontroller, the overall cost of using the device is reduced, and limited

space is conserved. Therefore, there existed a need to provide a microcontroller having an n-bit

architecture with less than or equal to n pins and a method therefor.

## SUMMARY OF THE INVENTION

An object of the present invention is to provide a microcontroller having an n-bit

architecture with less than or equal to n pins coupled to the microcontroller and a method

therefor.

Another object of the present invention is to provide a microcontroller having an n bit

architecture with the number of I/O pins less than n and a method therefor.

Yet another object of the present invention is to provide a microcontroller package with

pins for performing multiple functions and a method therefor.

Still another object of the present invention is to provide a microcontroller with n-bit data

processing capability and fewer than n I/O pins and a method therefor.

## BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to the present invention, an Integrated Circuit (IC) package is disclosed

comprising, in combination, an IC chip with a microcontroller therein having an n-bit data bus,

and up to n pins electrically coupled to the microcontroller. The IC package further comprises

control register means coupled to the microcontroller for receiving enable and disable signals.

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Pin function configuration means are also included coupled to the control register means for determining a function for a corresponding one of the n pins. The pin function configuration means comprises at least one functional block means coupled to the control register means for determining a function for a corresponding pin. The pin function configuration means may comprise a plurality of the functional block means each coupled to the control register means and to a corresponding pin of the n pins for determining a different function for the corresponding one of the n pins. The control register means provides independent control line means to each functional block means for transferring to each function block means one of the enable and the disable signals. Only one of the functional block means per pin is enabled at a time by the enable signal to configure a corresponding pin for a function associated with the enabled functional block means. Each functional block means is coupled to a corresponding one of the n pins and to the microcontroller for transferring data between the corresponding pin and the microcontroller when a particular one of the functional blocks is enabled. Additionally, the n pins include a number of Input/Output (I/O) type pins less than n.

Alternatively, a method of operating an Integrated Circuit (IC) package is disclosed comprising the steps of providing an IC chip with a microcontroller therein having an n-bit data bus, and providing up to n pins electrically coupled to the microcontroller.

The foregoing and other objects, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiments of the invention, as illustrated in the accompanying drawing.

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## BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a simplified block diagram view of the IC microcontroller package having an n-bit data bus and n pins.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

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Referring to Figure 1, the IC package or package of the instant invention is shown and generally designated by reference number 10. IC package 10 comprises an IC chip 11 with a microcontroller core or simply microcontroller 12 therein having an n-bit Data Bus (DB), and up to n pins 34-38 electrically coupled to the microcontroller 12. The manner of fabricating IC

70 packages 10, chips 11, and microcontrollers 12 are well known to those skilled in the art. Microcontroller 12 has, in general, an n-bit wide data bus, but more specifically here an 8-bit architecture or data bus width. Note that the data bus itself is not shown in detail for simplification of the drawing.

The IC package 10 further comprises a control register 16 coupled to the microcontroller

75 12 via a control signal bus 14 for receiving enable and disable signals from the microcontroller 12. Control registers are well known to those skilled in the art. The control register 16 can be any element that can hold a known state (i.e., charge, current, or voltage) such as SRAM, DRAM, EPROM, EEPROM, ROM, Combinational Logic, PROM, or the like. The control register 16 provides sufficient memory capacity to store and transfer the enable and disable

80 signals sent from the microcontroller 12 to the functional blocks 26, which will be described

later. The communications protocol for sending the enable and disable signals from the microcontroller 12 to the functional blocks 26 via the control register 16 is well known to those skilled in the art. The enable and disable signals are routed from the control register 16 to the appropriate functional blocks 26 via buses 18-24. From buses 22 and 24, each functional block 26 is coupled via connector 28 to receive the enable or disable signal sent from the control register 16. Note also that each functional block 26 has a connection 32 to a respective pin 34 to transfer data to or from the pin 34. Additionally, each functional block 26 has a connection 30 to the microcontroller 12 to transfer to or receive from the microcontroller 12 the appropriate data.

Note that pins 36 and 38 have no functional blocks 26 coupled thereto. This is because these pins 36 and 38 are the power and ground supply pins for the package 10, and therefore, they require no functional blocks 26. Note that the individual power and ground lines from pins 36 and 38 are not shown for simplification of the drawing. Pins 34 represent either input only or I/O type pins, both of which are well known in the art. Which of pins 34 are input only and which are I/O type depends on the user's application. Note that the second pin 34 from the top left corner of the package 10 only has one functional block 26 coupled to it. Thus, this particular pin 34 has only one function associated with it. Note that this single function depiction is shown only for the purpose of demonstrating how a single function pin 34 would look. Thus, any of the pins 34 could be single function pins, or multiple function pins 34. Additionally, note that the other pins 34 are shown with two functional blocks 26 per pin 34, and therefor these pins 34

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have two functions. In other words, the number of functions per pin 34 equals the number of functional blocks associated with that pin 34. Accordingly, any of the pins 34 could have one, two, or more functional blocks 26 associated thereto. This is represented in the drawing by the dashed lines between the functional blocks 26. Additionally note the dashed lines between pins 34, which indicate that this package 10 could have more or less than eight pins 34-38, but the key is that the number of pins 34-38 is less than or equal to the data bus width of the microcontroller 12.

The pin function configuration portion of the package 10 is defined as simply one or more functional blocks 26. The internals of the functional blocks 26 are not shown for simplification of the drawing. The functions that pins 34-38 must support for a microcontroller 12 are well known to those skilled in the art such as a Bi-Directional I/O Port pin, a Serial Programming Data pin, a Serial Programming Clock pin, and the like. The point is that there are many functions that pins 34-38 support for a microcontroller 12, they are all well known, and need not be specifically designated. Further, functional blocks 26, which enable a particular pin 34-38 to behave as required for a given function, are also well known in the art, and therefore need not be shown in detail. A key feature of the instant invention is that because pins 34 are multi-functional, only n pins 34-38 are required and all data control commands for the microcontroller 12 having an n-bit (i.e., 8-bit) data bus use the full n-bit bus.

## OPERATION

Referring to Figure 1, when executing an instruction, the microcontroller 12 sends appropriate control signals to the control register 16, which enables and disables the appropriate functional blocks 26 for a given pin 34. Note that since several functional blocks 26 can be used per pin 34, only one functional block can be enabled at a time. Data travels into the package 10 from a pin 34, through a corresponding connector 32, the enabled functional block 26, a corresponding connector 30, and to the microcontroller 12. The reverse path sends data from the microcontroller 12 out of a particular pin 34 of the package 10. Whether the flowpath of data be into or out of the microcontroller 12, the microcontroller 12 sends appropriate enable and disable signals to the appropriate functional blocks 26 in order to operate the desired pins 34 as required.

Although the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that changes in form and detail may be made therein without departing from the spirit and scope of the invention.

135    What is Claimed is:

1.    A method of operating an Integrated Circuit (IC) package comprising the steps of:

providing an IC chip with a microcontroller therein having an n-bit data bus; and

providing up to n pins electrically coupled to said microcontroller.

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2.    The method Claim 1 further comprising the step of providing control register means coupled to said microcontroller for receiving enable and disable signals.

3.    The method Claim 2 further comprising the step of providing pin function

145    configuration means coupled to said control register means for determining a function for a corresponding one of said n pins.

4.      The method of Claim 3 wherein the step of providing said pin function configuration means comprises the step of providing at least one functional block means coupled to said control register means for determining a function for a corresponding pin.

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5.      The method of Claim 4 wherein the step of providing said pin function configuration means comprises the step of providing a plurality of said functional block means each coupled to said control register means and to a corresponding pin of said n pins for determining a different function for said corresponding one of said n pins.

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6.      The method Claim 4 wherein the step of providing said control register means provides independent control line means to each functional block means for transferring to each function block means one of said enable and said disable signals.

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7.      The method of Claim 6 wherein only one of said functional block means per pin is enabled at a time by said enable signal to configure a corresponding pin for a function associated with said enabled functional block means.

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8.    The method of Claim 6 wherein each of said functional block means is coupled

to a corresponding one of said n pins and to said microcontroller for transferring data between

165    said corresponding pin and said microcontroller when a particular one of said functional blocks

is enabled.


9.    The method of Claim 1 wherein the step of providing up to said n pins includes

the step of providing a number of Input/Output (I/O) type pins less than n.

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10.    The IC package of Claim 1 wherein data control commands of said microcontroller

operate upon n-data bits.

FIG. 1

# DECLARATION

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*PATENT & TRADEMARK OFFICE*
*126*
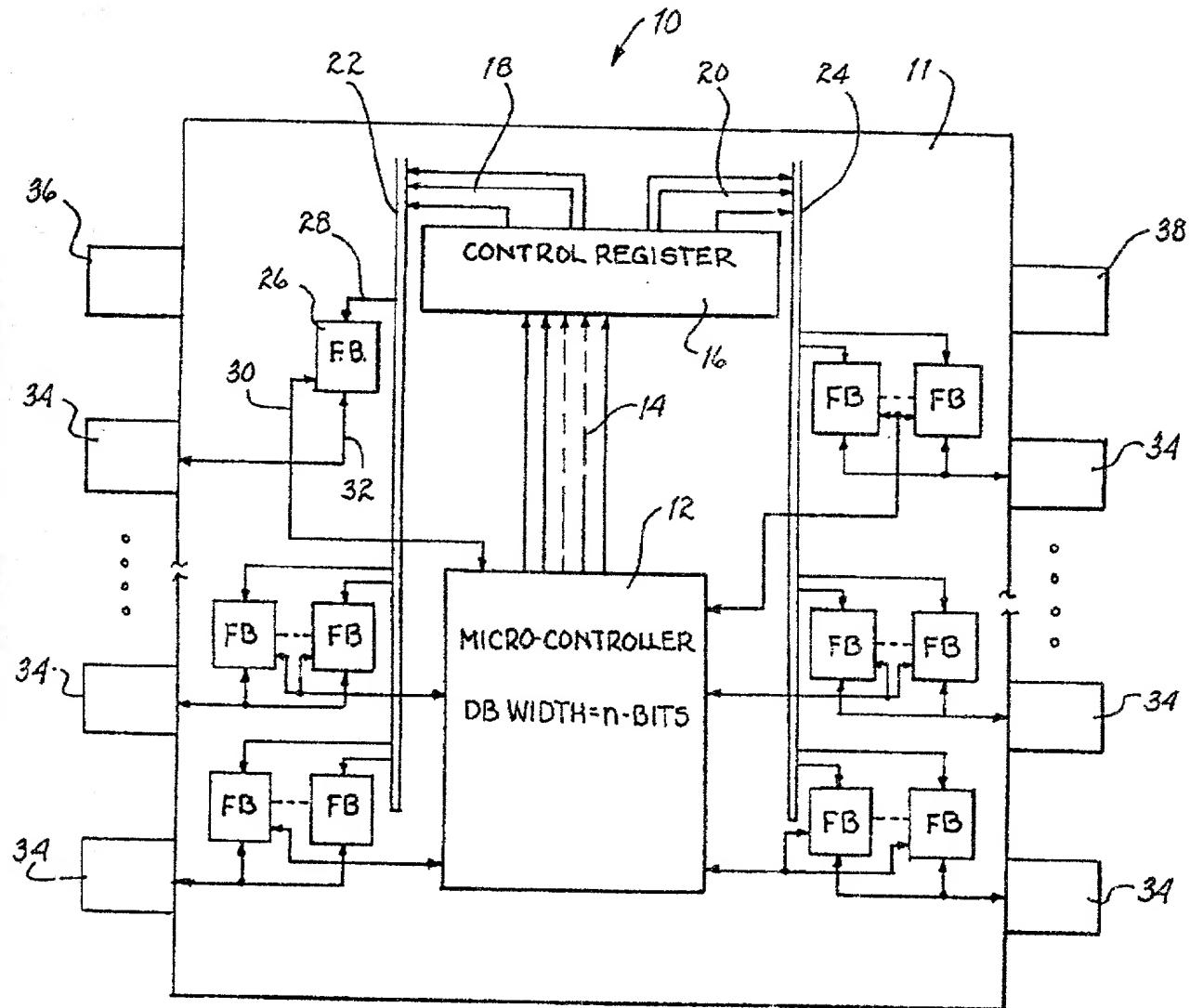
As a below named inventor. I hereby declare that: my residence, post office address, and citizenship are as stated below next to my name. I believe I am the original, first, and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

## A MICROCONTROLLER HAVING AN N-BIT DATA BUS WIDTH WITH LESS THAN N I/O PINS AND A METHOD THEREFOR

as described in the specification ☐ attached or ■ of Patent Application Serial No. 09/522,026 filed 10/08/98.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application; that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months prior to this application; and that I acknowledge the duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations § 1.56(a). Such information is material when it is not cumulative to information already of record or being made of record in the application, and

    (1)  it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
    (2)  it refutes, or is inconsistent with, a position the applicant has taken or may take in:
        (i)  opposing an argument of unpatentability relied on by the Office, or
        (ii)  asserting an argument of patentability.

I hereby claim foreign priority benefits under Title 35, United States Code § 119 of any foreign application(s) for patent or inventor's certificates listed below and have also identified below any foreign application(s) having a filing date before that of the application(s) on which priority is claimed:

| COUNTRY | APPLICATION NUMBER | DATE OF FILING | PRIORITY CLAIMED UNDER 35 USC 119 |
|---------|--------------------|----------------|-----------------------------------|
|         |                    |                | ☐YES   ■NO |

I hereby claim the benefit under Title 35 United States Code § 120 of any United States application(s) listed below and, insofar as any subject matter of any claim of this application is not disclosed in the prior United States Application, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

    Serial No. 08/644,916 filed May 24, 1996 – Patent No. 5,847,450

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

| FULL NAME OF FIRST JOINT INVENTOR | INVENTOR'S SIGNATURE | DATE |
|---|---|---|
| Scott Fink | *Scott Fink* | 7/18/00 |
| **RESIDENCE** 6327 Yucca, Glendale, AZ 85304 | | **CITIZENSHIP** U.S.A. |
| **POST OFFICE ADDRESS** 6327 Yucca, Glendale, AZ 85304 | | |

| FULL NAME OF SECOND JOINT INVENTOR | INVENTOR'S SIGNATURE | DATE |
|---|---|---|
| Gregory Bingham | *Gregory C. Bingham* | 7/24/00 |
| **RESIDENCE** 440 Bay Shore Blvd., Gilbert, AZ 85233 | | **CITIZENSHIP** U.S.A. |
| **POST OFFICE ADDRESS** 440 Bay Shore Blvd., Gilbert, AZ 85233 | | |

| FULL NAME OF THIRD JOINT INVENTOR | INVENTOR'S SIGNATURE | DATE |
|---|---|---|
| Richard Hull | Richard L. Hull | 7/21/00 |
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| 2138 W. Monroe Street, Chandler, AZ 85244 | | U.S.A. |
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| FULL NAME OF FOURTH JOINT INVENTOR | INVENTOR'S SIGNATURE | DATE |
|---|---|---|
| Scott Ellison | Scott Ellison | 7/18/00 |
| RESIDENCE | | CITIZENSHIP |
| 250 South Elizabeth Way, #2121, Chandler, AZ 85225 | | U.S.A. |
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| 250 South Elizabeth Way, #2121, Chandler, AZ 85225 | | |

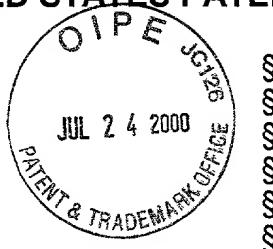# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

*Applicant/Patentee*: Scott Fink

*Filed*: 10/08/98

*Serial No.*: 09/522,026

*For*: MICROCONTROLLER HAVING AN N-BIT
    DATA BUS WIDTH LESS THAN N I/O PINS
    AND A METHOD THEREFOR

*Atty File*: M71462USD1

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## POWER OF ATTORNEY BY ASSIGNEE

Under the provisions of 37 C.F.R. § 3.71, the undersigned assignee of record of the entire interest in the above-identified patent/patent application by virtue of an assignment elects to conduct the prosecution of the application/maintenance of the patent to the exclusion of the inventor(s). The undersigned hereby declares that he has reviewed the above-referenced assignment and hereby declares that, to the best of his knowledge, title is in the Assignee, and further declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true. The assignee hereby revokes any previous powers of attorney and appoints the following to prosecute this application/maintain this patent and transact all business in the Patent and Trademark Office connected therewith:

| | | | |
|---|---|---|---|
| Ronald L. Chichester | 36,765 | R. William Beard, Jr. | 39,903 |
| Paul N. Katz | 35,917 | Paul R. Morico | 35,960 |
| Bruce W. Slayden, II | 33,790 | Catherine L. Bell | 35,444 |
| Ari O. Pramudji | 45,022 | Christopher J. Buntel | 44,573 |

Please direct all communications to: **Frohwitter, Three Riverway, Suite 500, Houston, Texas 77056 (713) 621-0703, Fax (713) 622-1624, to the attention of: Paul N. Katz.**

**ASSIGNEE**
MICROCHIP TECHNOLOGY INC.

Date: ___June 20, 2000___    BY: _____

NAME: Mary K. Simmons
TITLE: Vice President, General Counsel
      and Secretary

Please type a plus sign (+) inside this box ———▶ [+]

# CHANGE OF CORRESPONDENCE ADDRESS

*Application*

Address to:

Assistant Commissioner for Patents
Washington, D.C. 20231

| Application Number | 09/522,026 |
|---|---|
| Filing Date | October 8, 1998 |
| First Named Inventor | Scott FINK, et al. |
| Group Art Unit | 2508 |
| Examiner Name | |
| Attorney Docket Number | 068354.0161 |

Please change the Correspondence Address for the above-identified application to:

[X] Customer Number    | 023640 |    ———▶    *Place Customer Number Bar Code Label here*

*Type Customer Number here*

OR

| [X] Firm *or* Individual Name | Ronald L. Chichester |
|---|---|
| Address | Baker Botts L.L.P. |
| Address | 910 Louisiana Street |
| City | Houston, | State | TX | ZIP | 77002-4995 |
| Country | USA |
| Telephone | 713.229.1341 | Fax | 713.229.7741 |

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[ ] Applicant/Inventor.

[ ] Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

[X] Attorney or Agent of record.

[ ] Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number _____

| Typed or Printed Name | Ronald L. Chichester | Reg. No. 36,765 |
|---|---|---|
| Signature | *Ronald L. Chichester* | |
| Date | August 15, 2001 | |

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[ ] *Total of _____forms are submitted.

Burden Hour Statement: This form is estimated to take 3 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

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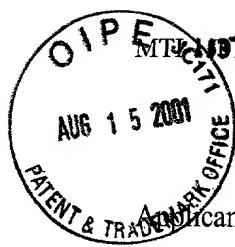
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| Applicant/Patentee: | | |
|---|---|---|
| FINK, et al. | § | Group Art Unit: 2508 |
| | § | |
| Serial No.: 09/522,026 | § | |
| | § | |
| Filed: OCTOBER 8, 1998 | § | Examiner: *To be Assigned* |
| | § | |
| Title: "A MICROCONTROLLER HAVING AN N-BIT DATA BUS WIDTH WITH LESS THAN N I/O PINS AND METHOD THEREFOR" | § | Atty File: 068354.0161 |

## POWER OF ATTORNEY BY ASSIGNEE

Under the provisions of 37 C.F.R. § 3.71, the undersigned assignee of record of the entire interest in the above-identified patent/patent application by virtue of an assignment recorded (check as applicable):

Concurrently Herewith
Date Recorded:
Reel/Frame:

elects to conduct the prosecution of the application/maintenance of the patent to the exclusion of the inventor(s). The undersigned hereby declares that he has reviewed the above-referenced assignment and hereby declares that, to the best of his knowledge, title is in the Assignee, and further declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true. The assignee hereby revokes any previous powers of attorney and appoints the following to prosecute this application/maintain this patent and transact all business in the Patent and Trademark Office connected therewith:

| R. William Beard, Jr.: 39,903 | Ronald L. Chichester: 36,765 | Claude E. Cooke, Jr.: 34,142 | Roger J. Fulghum: 39,678 |
|---|---|---|---|
| Michael A. Hawes: 38,487 | Carey J. Hetherington: 47,646 | Paul N. Katz: 35,917 | Michael G. Locklar: 44,878 |
| Mitchell D. Lukin: 30,772 | Jerry W. Mills: 23,005 | Paul R. Morico: 35,960 | Robert Neuner: 24,316 |
| Scott F. Partridge: 28,142 | Bruce W. Slayden, II: 33,790 | Howard L. Speight: 37,733 | Lori D. Stiffler: 36,939 |
| Khannan Suntharam: 45,144 | Melissa J. Szanto: 40,834 | G. Alan Witte: 36,061 | Joseph Uradnik: 36,955 |

Please direct all communications to: **Baker Botts L.L.P., One Shell Plaza, 910 Louisiana Street, Houston, Texas 77002-4995, 713.229.1343, Fax: 713.229.7743, attention of: Paul N. Katz.**

ASSIGNEE
MICROCHIP TECHNOLOGY INC.

DATE: August 10, 2001

BY: _____
NAME: Mary K. Simmons
TITLE: Vice President & General Counsel

HOU02:813540.1

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